Tier 1

* opus is much better at SPICE syntax
* chatgpt5 makes very sophisticated testbenches which are fully parameterized, sometimes even parameterizes the circuit under test
* chatgpt5 has more insightful design decisions, such as the decision to make the comparator input stage as both NMOS and PMOS
* chatgpt5 made a very strange mistake by making the output stage of the 2 stage OTA as NMOS, even though the input stage is also NMOS
* well known circuits are created well even if they are complicated, examples include current mirror and OTA and dual input stage comparator
* less known circuits do not work, even if the are simple, best example is source follower
* Opus is really bad in biasing circuits in general, but the circuit to be biased, for example the differential pair, works if correct biasing is applied
* Chatgpt5 sometimes makes strange decisions, like biasing tail current of differential pair with trivial ideal current source
* Opus creates less sophisticated circuits

Tier2

* Chatgpt5 fails hard at syntax
* Not a single chatgpt5 worked due to syntax
* Opus creates more working netlists but also with errors
* The 20 circuits had to be recreated using LTSPICE as schematics to really test them

So lets talk about the paper, here are my ideas in a semi random order

* The motivation is to see how useful LLMs are as is without any extra teaching or databases in analog circuit design
* There is previous work, but it all had some sort of RAG or prior teaching or something like this
* To the best of my knowledge this is the first work that tests the baseline of what LLMs can do as is in an in-context only scenario when in comes to analog circuit design
* Also this work publishes everything on Github to make everything transparent and available
* Also this work uses open source tools only to make everything reproducible
* The work is of course the first in many steps where we lay the foundation and in the coming work see what can be done to improve the performance using the results we found here
* The classification of the results in to three tiers aims to make them more specific, informative and insightful
* You will of course make more detailed analysis, but an important result in my opinion is the utter failure in producing clean SPICE netlists
* There are defeinitly knowledge gaps
* People complain that LLMs hallucinate when they write Python, they should check out what happens in a few lines of SPICE!
* And we tested two of the top models here.
* We still need schematics to make sense of the LLM output, this is definitely an area of research.

What do you think buddy? I am not finished, I am just brain dumping here and I will still continue my thoughts on the content and structure of the paper.

So here are some thoughts on the content and structure of the paper

* Introduction
  + Chip design is challenging
  + Analog circuit design is very challenging because the learning curve, need for experience, need from learning from masters and so on
  + Typical advanced analog circuit design does not rely on equations and the simplified MOSFET square law
  + Digital design is VHDL and Verilog based, i.e. programming language based and hence lends itself to generative AI implementation
  + Analog design is not like that at all
  + Previous work (need some thorguht referencing here, I have done some research using perplexity I can give you) has prior teaching or some sort of augmentation
  + No work on baseline capabilities
  + Motivation of this work is to test the native capabilities of state of the art commercial LLMs in in-context scenarios
  + The implications are important for designers and for teachers as well

What do you think so far?

So for the rest fo the paper:

* Method
  + Two models: chatgpt5 and Opus 4.1
  + In context-only
  + One shot prompt
  + 10 prompts for 10 circuits
  + No exchange, conversation, evaluate the outpt as is
  + Output divided into three tiers
    - Tier 1: one line explanation
    - Tier 2: one line explanation
    - Tier 3: one line explanation
* The prompts:
  + Chose 10 of the most common circuits and building blocks in analog design
  + Increasing order of complexity, from switch to 2 stage OTA and comparator
  + Typical specifications
* The PDK:
  + Simplified or abbreviated models of NMOS and PMOS of global foundries MCU 180nm 3.3 V
* The data and artifacts:
  + All available online in github

What do you think so far?

Now here is where I am a bit unsure how to proceed

* Should I proceed with the experiments per model
* Or should I proceed with the expermints
* Or should I proceed with the tier results

Do you know what I mean

* Like here are the results for chatgpt
* Then here are the results for opus
* And here is a comparison

Or

* Here are the results for circuit1
* Here are the results for circuit 2 till 10
* Here is a comparison and commentary

Or

* Here are the results for tier 1
* Here are the results for tier 2
* Here are the results for tier 3